# Article information:

Run-time power gating of on-chip routers using look-ahead routing | IEEE Conference Publication | IEEE Xplore
<https://ieeexplore.ieee.org/abstract/document/4484015>

# Article summary:

1. On-chip routers in Network-on-Chips play a key role in on-chip communication between cores, resulting in a larger standby power of routers compared with cores.

2. Run-time power gating of individual channels in a router is one of attractive solutions to reduce the standby power of chip without affecting the on-chip communication.

3. A sleep control method based on look-ahead routing is proposed to detect the arrival of packets two hops ahead, so as to hide the wake-up delay and reduce the short-term sleeps of channels.

# Article rating:

May be slightly imbalanced: The article presents the information in a generally reliable way, but there are minor points of consideration that could be explored further or claims that are not fully backed by appropriate evidence. Some perspectives may also be omitted, and you are encouraged to use the research topics section to explore the topic further.

# Article analysis:

The article provides an overview of run-time power gating for on-chip routers using look-ahead routing, and presents a proposed sleep control method based on this approach. The article is well written and provides sufficient detail about the topic, including an analysis of power consumption for a typical on-chip router architecture and an evaluation of the proposed sleep control method.

The article does not appear to be biased or partial towards any particular point of view, as it presents both sides equally and does not make unsupported claims or omit counterarguments. It also does not contain any promotional content or present risks without noting them.

The only potential issue with the article is that it does not explore all possible counterarguments or points of consideration related to run-time power gating for on-chip routers using look-ahead routing. For example, it does not discuss potential drawbacks or limitations associated with this approach such as increased complexity or cost. Additionally, while it provides an evaluation of the proposed sleep control method, it does not provide evidence for its claims regarding improved performance or reduced power consumption compared to other methods.

# Topics for further research:

* Drawbacks of run-time power gating
* Limitations of look-ahead routing
* Comparison of power gating methods
* Impact of power gating on router performance
* Cost of on-chip router power gating
* Power consumption of on-chip routers

# Report location:

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