# Article information:

MP3: Minimizing performance penalty for power-gating of Clos network-on-chip | IEEE Conference Publication | IEEE Xplore
<https://ieeexplore.ieee.org/abstract/document/6835940>

# Article summary:

1. Power-gating is a promising technique to reduce static power of on-chip routers.

2. Clos networks are good targets for power-gating due to their path diversity and decoupling between processing elements and most of the routers.

3. MP3 (Minimal Performance Penalty Power-gating) is proposed as an effective power-gating scheme which can achieve minimal performance penalty and save more static energy than conventional power-gating applied to Clos networks.

# Article rating:

May be slightly imbalanced: The article presents the information in a generally reliable way, but there are minor points of consideration that could be explored further or claims that are not fully backed by appropriate evidence. Some perspectives may also be omitted, and you are encouraged to use the research topics section to explore the topic further.

# Article analysis:

The article provides a detailed overview of the potential benefits of applying power-gating techniques to Clos networks, as well as the proposed MP3 (Minimal Performance Penalty Power-gating) scheme for achieving minimal performance penalty while saving more static energy than conventional power-gating. The article is well written and provides a comprehensive overview of the topic, with clear explanations and examples provided throughout. The authors provide evidence from full system evaluation using PARSEC benchmarks to support their claims, which adds credibility to the article.

However, there are some potential biases in the article that should be noted. For example, the authors focus solely on the benefits of applying power-gating techniques to Clos networks without exploring any potential drawbacks or counterarguments that could be raised against this approach. Additionally, there is no discussion of possible risks associated with this approach or how these risks could be mitigated. Furthermore, while the authors provide evidence from full system evaluation using PARSEC benchmarks, it would have been beneficial if they had also provided evidence from other sources such as real world applications or simulations in order to further strengthen their argument.

In conclusion, while this article provides a comprehensive overview of the potential benefits of applying power-gating techniques to Clos networks and presents evidence from full system evaluation using PARSEC benchmarks in support of its claims, there are some potential biases that should be noted such as lack of exploration into counterarguments or possible risks associated with this approach and lack of evidence from other sources such as real world applications or simulations.

# Topics for further research:

* Power-gating techniques drawbacks
* Power-gating techniques risks
* Real world applications of power-gating techniques
* Simulations of power-gating techniques
* Counterarguments to power-gating techniques
* Mitigation of risks associated with power-gating techniques

# Report location:

<https://www.fullpicture.app/item/571fca285c11e76376307d631273b5e4>