# Article information:

NoRD: Node-Router Decoupling for Effective Power-gating of On-Chip Routers | IEEE Conference Publication | IEEE Xplore  
<https://ieeexplore.ieee.org/abstract/document/6493626>

# Article summary:

1. The paper proposes NoRD (Node-Router Decoupling), a novel power-aware on-chip network approach that provides for power-gating bypass to decouple the node's ability for transferring packets from the powered-on/off status of the associated router.

2. Simulation shows that NoRD can substantially reduce the number of state-transitions, completely hide wakeup latency from the critical path of packet transport and eliminate node-network disconnection problems.

3. Compared to an optimized conventional power-gating technique applied to on-chip routers, NoRD can further reduce the router static energy by 29.9% and improve the average packet latency by 26.3%, with only 3% additional area overhead.

# Article rating:

May be slightly imbalanced: The article presents the information in a generally reliable way, but there are minor points of consideration that could be explored further or claims that are not fully backed by appropriate evidence. Some perspectives may also be omitted, and you are encouraged to use the research topics section to explore the topic further.

# Article analysis:

The article is overall reliable and trustworthy in its claims and evidence presented. The authors provide a detailed description of their proposed approach, NoRD (Node-Router Decoupling), as well as simulations and full system evaluations using PARSEC benchmarks to support their claims about its effectiveness in reducing energy consumption and improving performance. The authors also note potential risks associated with their approach, such as increased area overhead, but they are able to demonstrate that these risks are minimal compared to the benefits provided by NoRD. Furthermore, they provide a thorough discussion of related works in this field, which helps to put their work into context and demonstrate how it builds upon existing research in this area.

The only potential issue with this article is that it does not explore any counterarguments or alternative approaches to solving this problem; however, given that this is a conference publication rather than a journal article, it may be assumed that such exploration was done elsewhere prior to submitting this paper for publication.

# Topics for further research:

* Energy-efficient computer architecture
* Network-on-chip design
* Dynamic voltage and frequency scaling
* Power-aware routing algorithms
* Network-level optimization techniques
* Low-power embedded systems

# Report location:

<https://www.fullpicture.app/item/7aa480f5edcb0f05850ba2d526117946>