# Article information:

Theoretical Study for Carrier Transit Limited Performance of Gate-All-Around Si Nanowire Transistor by Time-Dependent Quantum Transport Simulation | IEEE Journals & Magazine | IEEE Xplore
<https://ieeexplore.ieee.org/document/9925998>

# Article summary:

1. This article explores the upper limit performance of gate-all-around (GAA) Si nanowire transistors by using time-dependent quantum transport simulation.

2. The transient characteristics of channel charge are investigated, and it shows the response time of channel charge is in the scale of 0.1 ps.

3. The carrier transit limited performance including the frequency-dependent gate capacitance and transconductance, 3 dB bandwidth, and cutoff frequency, are calculated and discussed.

# Article rating:

May be slightly imbalanced: The article presents the information in a generally reliable way, but there are minor points of consideration that could be explored further or claims that are not fully backed by appropriate evidence. Some perspectives may also be omitted, and you are encouraged to use the research topics section to explore the topic further.

# Article analysis:

The article is generally reliable as it provides a comprehensive overview of the theoretical study for carrier transit limited performance of GAA Si nanowire transistors by time-dependent quantum transport simulation. It presents a detailed analysis of the transient characteristics of channel charge, as well as an exploration into the carrier transit limited performance including frequency-dependent gate capacitance and transconductance, 3 dB bandwidth, and cutoff frequency. Furthermore, it cites relevant research to support its claims such as Di et al., Ahn and Hong, Goel et al., Kushwaha et al., Lin et al., which adds to its credibility.

However, there are some potential biases that should be noted in this article. For example, it does not present both sides equally when discussing the upper limit performance of nanoscale transistors; instead it focuses solely on GAA Si nanowire transistors without exploring other types of nanoscale transistors such as FinFETs or CNTFETs. Additionally, there is no mention of possible risks associated with this type of transistor or any counterarguments that could be made against its use in future nanotechnology applications. Finally, there is a lack of evidence for some claims made in the article such as how good the transistor can be if one can minimize non-ideal factors; more evidence should be provided to support these claims.

# Topics for further research:

* FinFETs performance comparison
* CNTFETs performance comparison
* Nanoscale transistor risks
* Non-ideal factors in GAA Si nanowire transistors
* Upper limit performance of nanoscale transistors
* Counterarguments against GAA Si nanowire transistors

# Report location:

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